Intel's Mobility Technology

Designing for a Mobile World

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VP & GM Mobile Microprocessors Group
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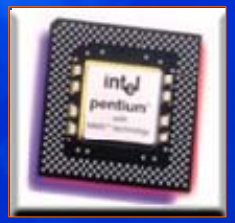
Topics

- IDC Development Evolution
- Enabling the Vectors of Mobility
- Evolution of Intel Centrino Mobile Technology
- Developing for Performance/Power
  - Yonah / Merom
- Summary

IDC Evolution

Growth

Pentium MMX™
- A Microprocessor
- Innovative arch
- Sold in 10s of Mu
- Owner of complete product development
- Increased influence
- In the corp mainstream



CMT
- Biz Focus
- Unique & differentiated value proposition
- Four Mobility Vectors
- Excellent Execution
- In the center of influence
- Platform solution which benefits from Intel's strengths

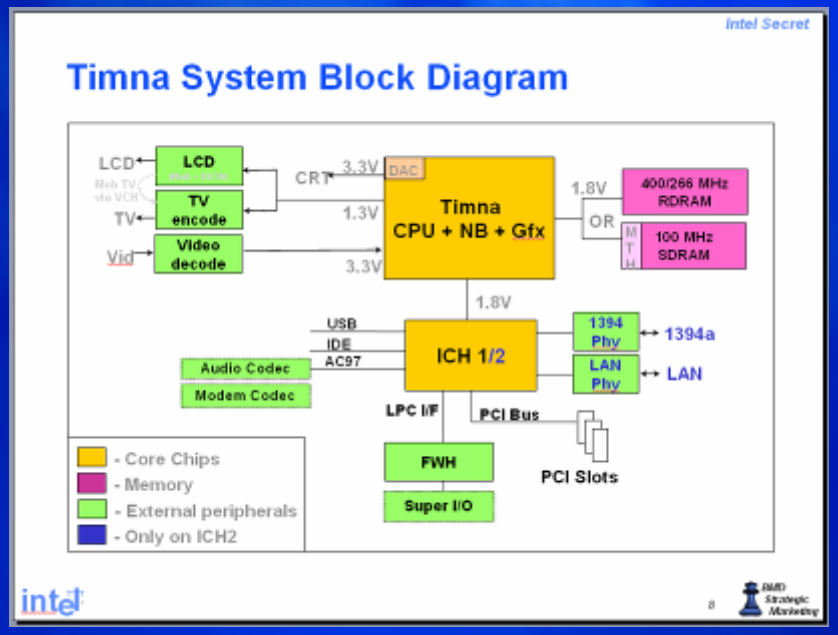
Timna

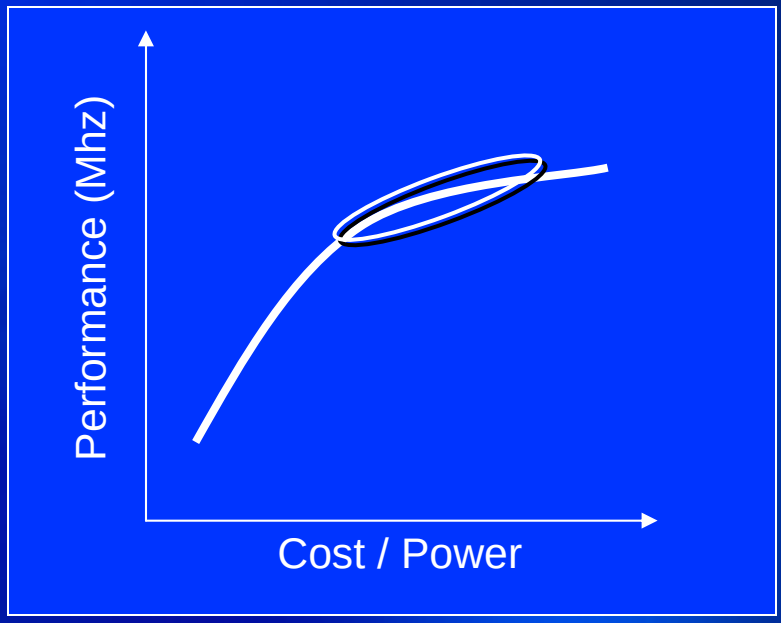
The 80s
- Design focus
- Many eggs in a basket strategy
- Opportunistic – "design for hire"
- No clear strategy
- Tech Leadership

Time

* Source: Andy Grove, *Only the Paranoid Survive*

Timna Experience





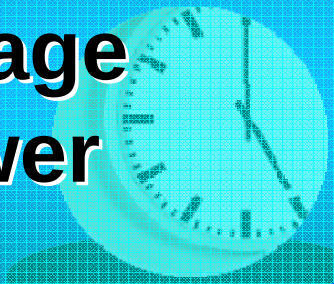
- Originally planned as PC value product
- Changed the paradigm of pushing performance / frequency at all cost
- Product was unsuccessful due to cost of RDRAM
- Learned few important facts about performance / power

Enabling the 4 Vectors – CPU Impact

Wireless Capability

Enables Great Battery Life

Average Power

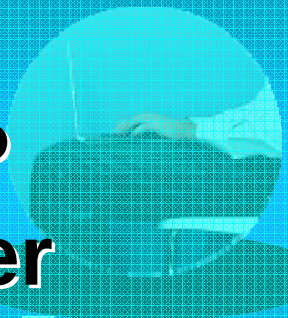


Power Per Performance

Mobile Performance

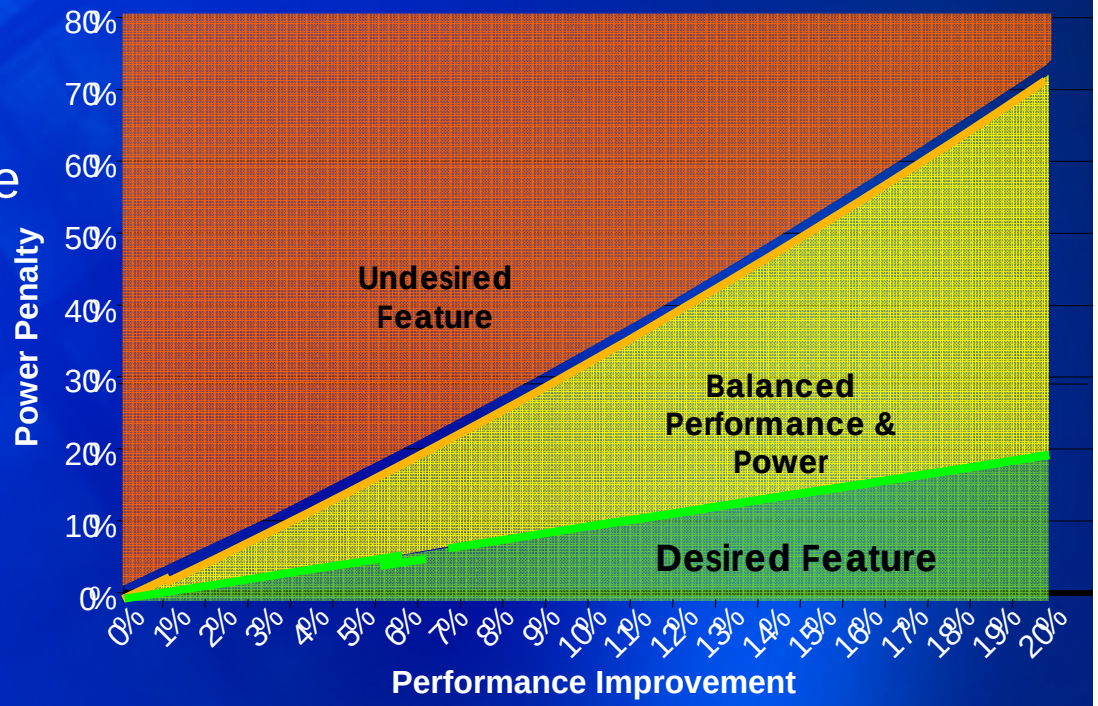
TDP Power

Sleek Form Factor



Banias Design Approach

- Replace performance by power per performance
- Focus on active and in-active power reduction when hardware resource is:
  - highly loaded
  - idle

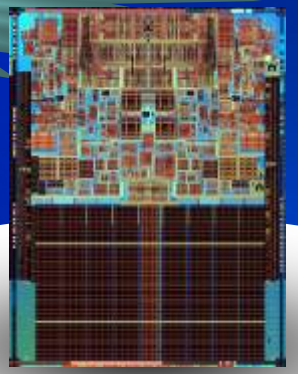


Achieving High Performance with Lower Power

Evolution of Intel's Next Generation Micro-Architecture

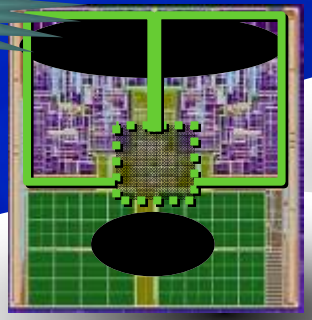
Intel® Smart Cache
Dynamic Power Coordination
Advanced Thermal Manager

Merom



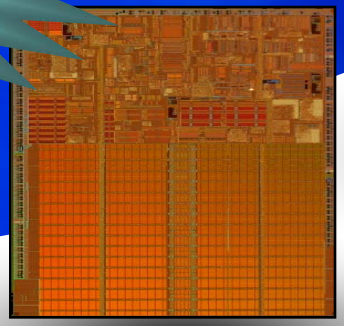
2MB Power
rficient L2 Cache

Yonah

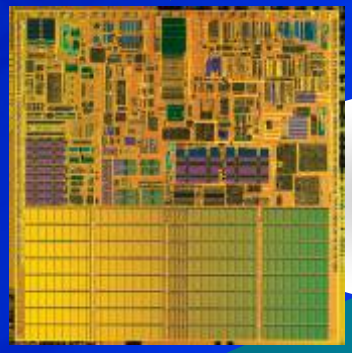


Enhanced
SpeedStep® Technology
400 MHz Power
Optimized System Bus

Dothan



Banias



2003

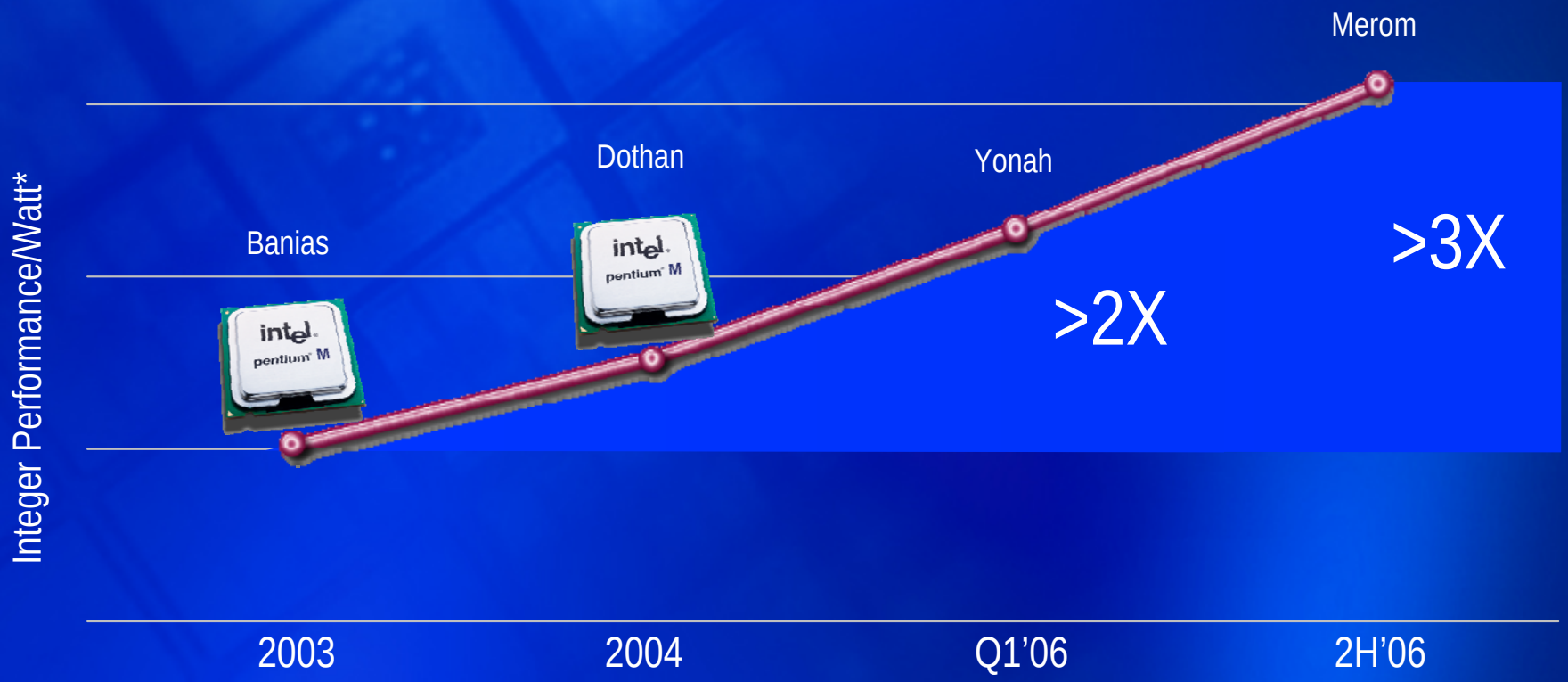
2004

2005

2006

Continuous improvement

Driving Performance/Watt

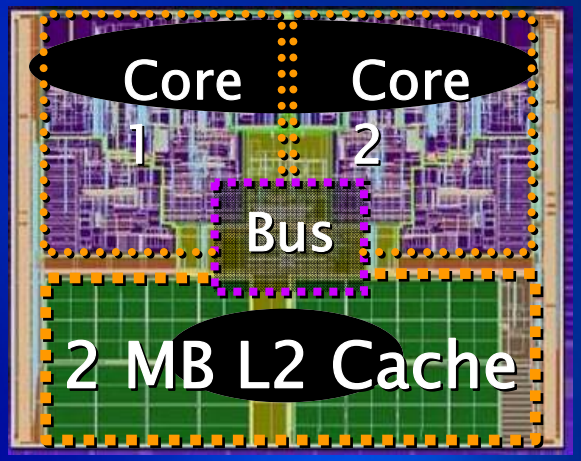


*SpecIntRate

Yonah Dual-Core Processor with Intel® Smart Cache

Intel® Smart Cache

- Both Cores can use the full size Shared L2
- Shared Data can be accessed from cache minimizing bus traffic
- New L1 & L2 data pre-fetchers and deeper write buffers
- Centralized control logic enables power optimization and power saving

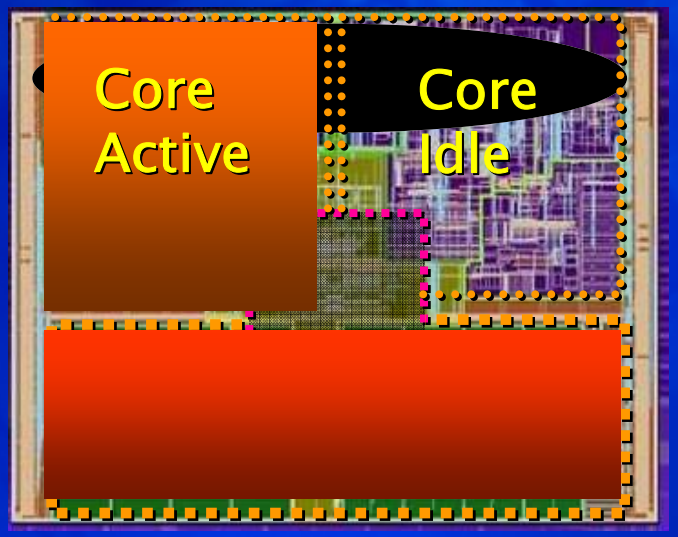


Smarter and Efficient Cache Design enables better Performance, Responsiveness & Power Savings

Yonah: Intel® Smart Cache

Dynamic Cache Allocation

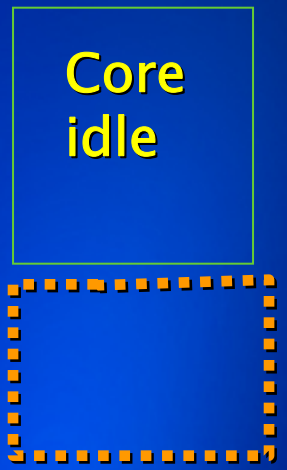
Intel® Smart Cache



Shared L2 enables active execution core to access full cache when one other execution core is idle

Split-Cache Dual-Core Design

Performance loss due to increased cache misses

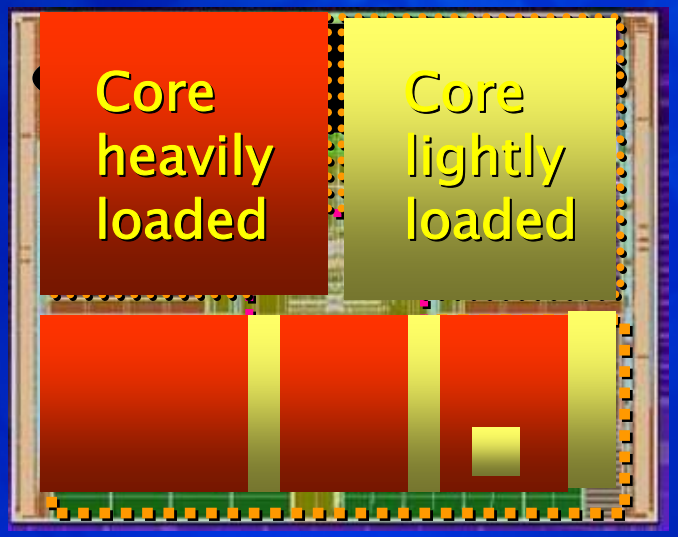


Cache not utilized

Yonah: Intel® Smart Cache

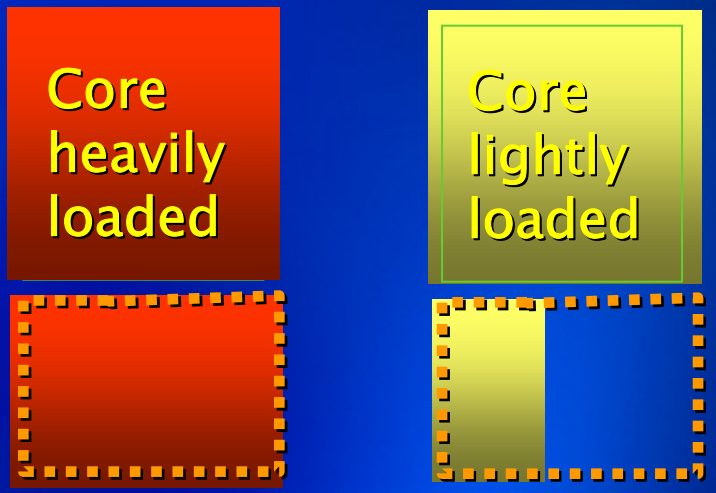
Dynamic Cache Allocation

Intel® Smart Cache



Shared L2 enables each execution core to access shared cache based on application and performance needs

Split-Cache Dual-Core Design



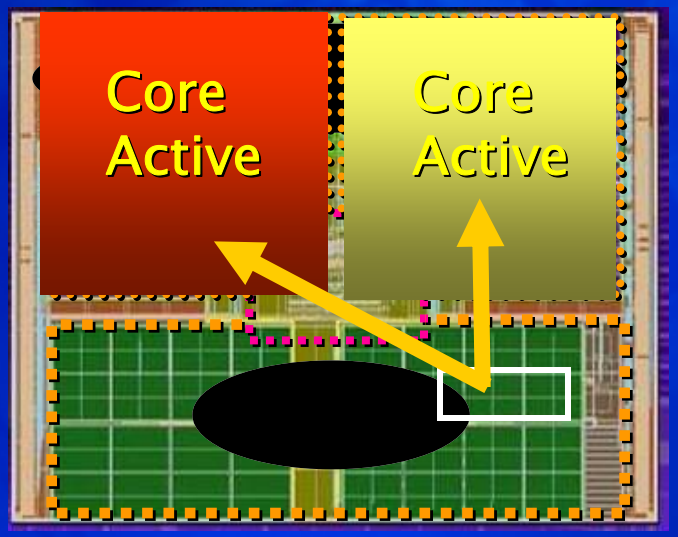
Performance loss due to increased cache misses

Cache under-utilized

Yonah: Intel® Smart Cache

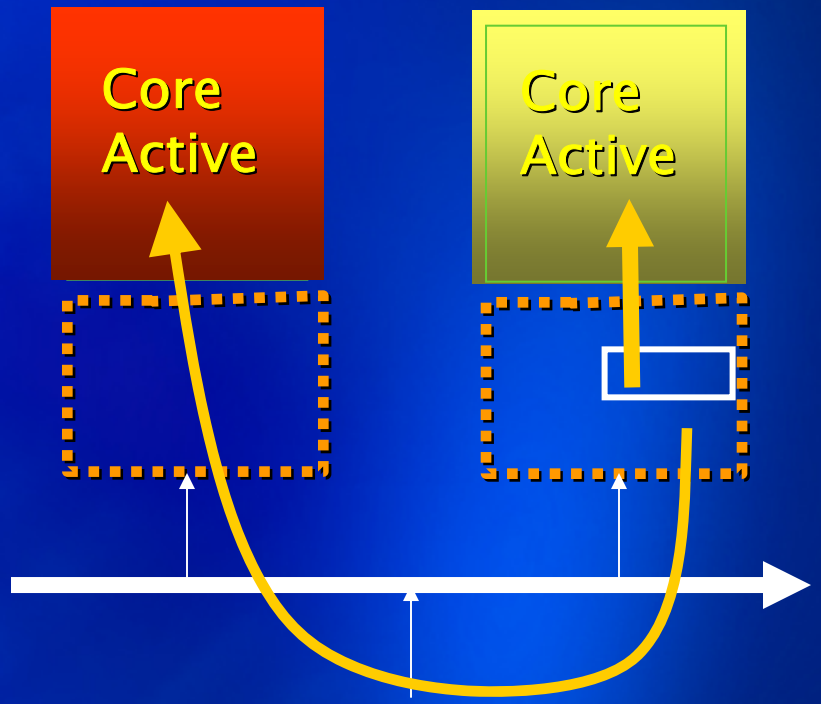
Efficient Data Sharing

Intel® Smart Cache



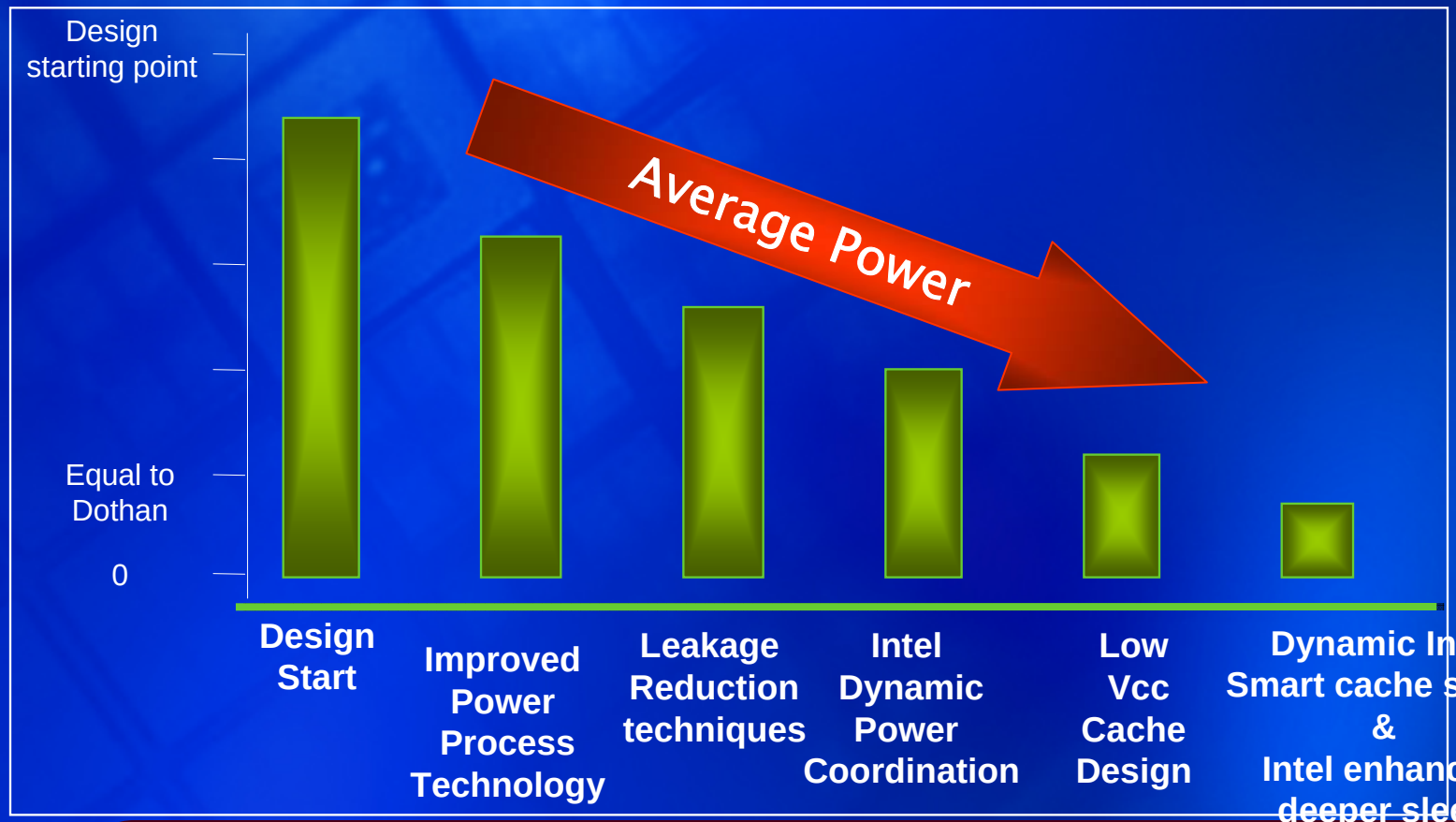
Shared L2 minimizes front side bus traffic and reduces control logic complexity

Split-Cache Dual-Core Design



Performance loss and increase in power

Extending Battery Life while doubling the amount of transistors



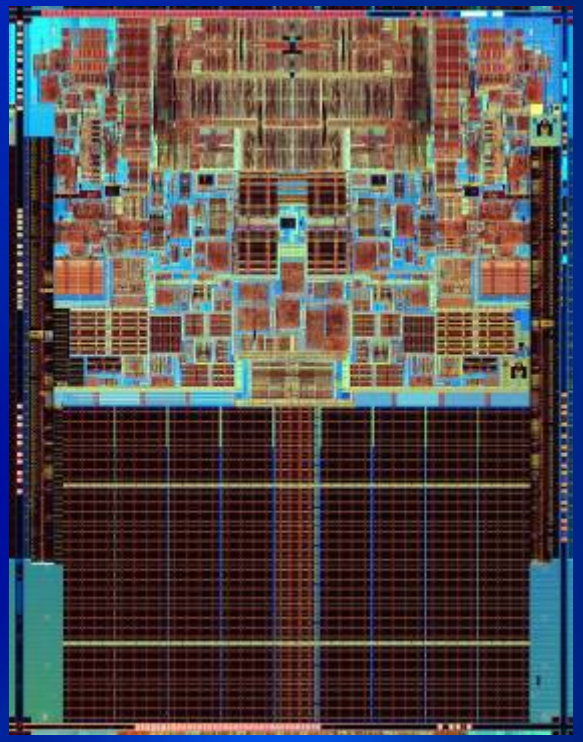
Maintaining average power while delivering increased performance with dual-core

Extending Battery Life by Managing L2 Cache

- Cache is a significant element of average power
  - Turn cache off whenever possible
  - Maintain data integrity and memory coherency
- Cache data retention is the limiter to lower voltage (Vcc_Min)
- Yonah introduces three new mechanisms to manage cache voltage and power
  - Dynamic Intel® Smart Cache sizing
  - Enhanced Intel® Deeper Sleep
  - Low Vcc Cache Design

Intel's Next Generation Micro-Architecture

- Foundation for future IA-32 platforms
  - Merom - 1st mobile
  - Conroe - 1st Desktop
  - Woodcrest - 1st server
- Low power, high performance, scaleable
- New features
  - Wider instruction/decode issue engine and more powerful execution units
  - Higher FSB speed
  - Improved memory sub system bandwidth
  - Enhanced instruction fusion
  - E64T
  - New instructions for media performance



Summary

- Innovation is sometimes born in unplanned manner
- We adopt the approach of continuous improvement rather than “big bang”
- Multi-core era brings new challenges which require new innovation

Thank you!

Questions?

Extending battery life
Dynamic Intel® Smart Cache Sizing

- HW based algorithm predicts the cache usage requirements
  - Considers the % of time the CPU is in active state vs. various sleep states
  - Guided by OS through Mwait command
- During periods of low activity or inactivity Yonah dynamically adapts its effective cache size
  - Cache content is gradually synced with system memory
  - Cache ways are being turned off (physically as well as logically), thus reducing power
- Cache is re-powered to deliver full performance on demand